

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/710,066	NORMOYLE, KEVIN B.	
Examiner R. Stephen Dildine		Art Unit 2133	Page 1 of 1	

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 03186954 A	08-1991	Japan	KANEKO et al.	G06F 12/16
	O	WO 9002372 A1	03-1990	WIPO	SCHEUNEMAN et al.	G06 F 11/10
	P	JP 2000099409 A	04-2000	Japan	MUKAI, HIROAKI	G06F 12/16
	Q	JP 05181757 A	07-1993	Japan	KUBOYA, MAKOTO	G06F 12/16
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Bergey, A. L.; Checking Algorithm for Two Byte RAM with One or Two Byte Access; 1 April 1994; IBM Technical Disclosure Bulletin, Vol 37, No. 04B; pages 655-658
	V	Henle, et al.; Error Correcting Address Technique; 1 May 1970; IBM Technical Disclosure Bulletin, Vol 12, No. 12, pages 2071-2072
	W	Kaufman, D. R.; Address Error Detection for Memory Using SEC/DED with Processor Using Byte Parity Error Detection; 1 April 1982; IBM Technical Disclosure Bulletin, Vol 04, page 6122
	X	Derwent abstract of inventor's certificate SU 1501122 A (Ivakhiv et al.)

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.